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10/647,064	08/22/2003	Paul Moroney	D03037	9712

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EXAMINER	
TRAN, ELLEN C	

ART UNIT	PAPER NUMBER
2433	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Docketing.Mobility@motorola.com

Office Action Summary	Application No.	Applicant(s)	
	10/647,064	MORONEY ET AL.	
	Examiner	Art Unit	
	ELLEN TRAN	2433	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2010*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This action is responsive to communication filed on: 5 November 2010. The original application filed was filed on 22 August 2003, with acknowledgement of priority date of 23 August 2002, based on provisional application filing of 60/405,537.

2. Claims 30-54, are pending; claims 30, 41, and 47 are independent claims. Claims 30, 41, and 47, have been amended. Claims 53 and 54 are new. Amendments to the claims are accepted. The 101 rejection is removed due to amendment.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed 5 November 201has been entered.

Response to Arguments

4. Applicant's arguments filed 5 November 2010 have been fully considered however they are moot due to new grounds of rejection initiated by applicant's amendment to the independent claims or are not persuasive where noted below.

I) In response to applicant's argument II Claim Objections, "such rule is not a "should" (mandatory rule typically use the term "must" or "shall"). Hence, such a rule is not a basis upon which an objection can be made to compel action from Applicant".

The Examiner disagrees and notes it is only an Objection therefore the objection is maintained.

II) In response to Prior Art Rejections, "Neither Coli nor Candelore '489 taken alone or in combination disclose or suggest the claimed invention recited by the above amended claims"

This argument is moot because newly introduced prior art Maruo teaches the amended portions of the claims as best understood.

III) In response to Applicant's argument, "Neither Coli nor Candelor '489 appear to be related to interchip data protection … Coli does not protect interchip communications. At best, Coli provides for a non-readable and non-rewritable IC".

The Examiner disagrees with argument. The Applicant's at best summary of Coli are protecting interchip communications. First an IC is a chip. Second if an IC is non-readable or non-rewritable the interchip communications are protected.

IV) In response to Applicant's argument, "As explained in Applicant's previous response, Candelor '489 is also not concerned with interchip content protection. Candelor '489 uses a smart card (410) to control words, which are then sent to a second device (401 under encryption through an interface 420 … Such discussion does not relate to interchip content pathways".

The Examiner disagrees with argument. Candelor '489 was used to reject claim limitations "a second chip package, wherein the second chip package comprises: a second body, a decryption engine, and a second key storage register capable of storing the interchip key ..." Since the content within a smartcard is protected Candelor does protect 'interchip content pathways'.

Claim Objections

5. Claims 30-54 are objected to because of the following informalities: According to 37 CFR 1.75 Claims (g) and MPEP 608.01(e) [R-3] the independent claims should be presented in

order, with the least restrictive claim to be presented as claim number 1. In the interest of compact prosecution the Examiner finds Applications with the claims presented in the proper order make it easier to determine allowable subject matter. Independent claims 41 and 47 are less restrictive than claim 30. Appropriate correction is required.

6. Claims 30-54 are objected to because of the following informalities: the amended claim end with "eachother" with no space between the words. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 30-54 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended claims contain the phrase "wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother". The original disclosure did not contain this limitation.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 30-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The amended claims contain the phrase "wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother".

First it is not clear what the Applicant is defining as 'a single device'.

Second the claims state "a second chip package … the interchip key is used by the decryption engine to produce plaintext content from the ciphertext content received from the first chip package". If there is not interface between the first and second chip packages how is "ciphertext content received from the first chip package".

11. To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. 112 above are further rejected as set forth below in anticipation of applicant amending these claims to overcome the 112 rejection.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 30-54,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Coli U.S. Patent No. 5,452,355 (hereinafter '355) in view of Candelore U.S. Patent No. 6,697,489 (hereinafter '489) in further view of Maruo et al. U.S. Patent 7,146,007 (hereinafter '007).

As to independent claim 30, "A content processing unit for protecting interchip content pathways transporting content, the content processing unit comprising: a first chip package which receives content, wherein the first chip package comprises: a first body, an encryption engine, and a first key storage register capable of storing an interchip key, wherein:" is taught in '355 col. 1, lines 45-59;

"the first key storage register is non-readable from outside the first body, and" is shown in '355 col. 2, lines 3-25;

"the first key storage register cannot be overwritten after a programmability period" is disclosed in '355 col. 4, lines 8-52;

the following is not explicitly taught in '355:

"the interchip key is used by the encryption engine to produce ciphertext content from the received content" however '489 teaches that encryption engines with interchip keys are used to produce ciphertext context in col. 5, lines 57-62;

"the programmability period being a period in which the interchip key is loaded in the first key storage" however '489 teaches that these interchip keys are programmed at the time of manufacture in col. 7, lines 1-10;

"a second chip package, wherein the second chip package comprises: a second body, a decryption engine, and a second key storage register capable of storing the interchip key, wherein: the interchip key is used by the decryption engine to produce plaintext content

from the ciphertext content received from the first chip package, and the second key storage register is non-readable from outside the second body, the second key storage register being writeable while being non-readable; and an interchip content pathway connecting the first chip package and the second chip package within said content processing unit, the interchip content pathway carrying the ciphertext content from the first chip package to the second chip package; and an output configured to provide the plaintext content to a user device capable of providing content to a user" however '489 teaches a smartcard (i.e. second chip package) is used with a conditional access module to decrypt content received and how the secure content is protected by using the secure keys in col. 6, lines 27-58;

It would have been obvious to one of ordinary skill in the art at the time of the invention of a tamper protection cell taught in '355 to utilize the tamper protection cells in a traditional conditional access system such as television distribution. One of ordinary skill in the art would have been motivated to perform such a modification because smartcards (i.e. tamper protection cells use with the distribution of television content is well known in the prior art see '489 (col. 2, line 45 through col. 3, line 9).

the following is not explicitly taught in '355 and '489**: "wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother"** however '007 teaches a secure path with a first functional block and s second functional block where the signal cannot be intercepted in the Abstract as well as col. 3, lines 41-59.

It would have been obvious to one of ordinary skill in the art at the time of the invention of a tamper protection cell taught in '355 and '489 to protect content between chip packages. One of ordinary skill in the art would have been motivated to perform such a modification because the prior art system provide opportunities for the content to be pirated see '007 (col. 2, lines 5-67).

As to dependent claim 31, "further the first chip package includes a fusable link, wherein the first key storage register cannot be overwritten after the fusable link is activated" is taught in '355 col. 4, lines 8-52.

As to dependent claim 32, "wherein the programmability period ends after writing to the first key storage register" is shown in '490 col. 7, lines 1-10.

As to dependent claim 33, "wherein at least one of the first and second chip packages comprises a plurality of semiconductor substrates" is disclosed in '355 col. 1, lines 31-37 and col. 4, lines 40-42.

As to dependent claim 34, wherein: the first chip package further stores a key encryption key, the interchip key is encrypted with the key encryption key, and the second chip package obtains the interchip key by decrypting the interchip key using the key encryption key" is taught in '489 col. 6, lines 27-36, note the second chip package in this embodiment is interpreted to be the unique descrambler IC key stored in register 450, and the first chip package is the smartcard.

As to dependent claim 35, "further comprising a plurality of content processing chip packages, each content processing chip package of the plurality of content processing chip packages having a unique key as the key encryption key, the unique key of each content

processing chip package being distinct from the unique key of each other content processing chip package" is shown in '489 col. 7, lines 11-19, note because it is a manufacturing process there are a plurality of smart cards that are paired with a respective plurality of to a specific host Descrambler IC.

As to dependent claim 36, "wherein each of the plurality of content processing chip packages receives a ciphertext message and obtains a unique interchip key by using the unique key to decrypt the message, the unique interchip key of each content processing chip package being distinct from the unique interchip key of each other content processing chip package" is taught in '489 col. 7, lines 15-20.

As to dependent claim 37, "wherein the second key storage register is overwritable" is shown in '489 col. 7, lines 15-20.

As to dependent claim 38, "wherein: the second chip package further comprises a second encryption engine, and the second encryption engine uses the interchip key or another key that is a function of the interchip key" is taught in '489 col. 7, line 59 through col. 8, line 19.

As to dependent claim 39, "further comprising a third chip package comprising a second interchip key that can decrypt second ciphertext content produced with the second encryption engine at the second chip package" is shown in '489 col. 7, lines 59-65.

As to independent claim 40, "wherein the third chip package is connected to the second chip package by a second interchip content pathway, the second interchip content pathway carrying the second ciphertext content from the first chip package to the second chip package" is taught in '489 col. 7, lines 15-20, i.e. third equivalent to replaced.

As to independent claim 41, "A method for protecting interchip content pathways transporting content within a content processing unit, the method comprising steps of: encrypting digital content at a first chip package with an interchip key to produce ciphertext content" and "wherein the interchip key in the first key storage register is non-readable from outside the first chip package" is taught in '355 col. 1, lines 45-59 and col. 4, lines 8-52;

the following is not explicitly taught in '355:

"the interchip key being previously loaded into a first key storage register in a first chip package" however '489 teaches that keys are programmed at the time of manufacture in col. 7, lines 1-10;

"encrypting digital content with the interchip key to produce ciphertext content" however '489 teaches that encryption engines with interchip keys are used to produce ciphertext context in col. 5, lines 57-62;

"coupling the ciphertext content from the first chip package to an interchip content pathway" however '489 teaches coupling chip packages in a content pathway, i.e. interface in col. 5, line 57 through col. 6, line 4;

"coupling the ciphertext content from the interchip content pathway to a second chip package; and decrypting the ciphertext content with the interchip key to reformulate the digital content" however '489 teaches a smartcard (i.e. second chip package) is used with a conditional access module to decrypt content received and how the secure content is protected by using the secure keys in col. 6, lines 27-58

"wherein the interchip key was previously loaded into a second key storage register in the second chip package" however '489 teaches that keys are programmed at the time of manufacture in col. 7, lines 1-10

"wherein the interchip key in the second key storage register is non-readable from outside the second chip package, the second key storage register being writable while being non-readable, and" however '489 teaches the use of a smartcard to process encrypted content, key storage register of smartcard are non-readable in addition as shown in '489 a key is programmed into the smartcard in col. 7, lines 1-10;

It would have been obvious to one of ordinary skill in the art at the time of the invention of a tamper protection cell taught in '355 to utilize the tamper protection cells in a traditional conditional access system such as television distribution. One of ordinary skill in the art would have been motivated to perform such a modification because smartcards (i.e. tamper protection cells use with the distribution of television content is well known in the prior art see '489 (col. 2, line 45 through col. 3, line 9).

the following is not explicitly taught in '355 and '489**: "wherein the first chip package, the second chip package and the interchip content pathway are contained in a single device without an interface between eachother"** however '007 teaches a secure path with a first functional block and s second functional block where the signal cannot be intercepted in the Abstract as well as col. 3, lines 41-59.

It would have been obvious to one of ordinary skill in the art at the time of the invention of a tamper protection cell taught in '355 and '489 to protect content between chip packages. One of ordinary skill in the art would have been motivated to perform such a modification

because the prior art system provide opportunities for the content to be pirated see '007 (col. 2, lines 5-67).

As to dependent claim 42, "further comprising steps of: loading a key encryption key into the first chip package; and decrypting the interchip key with the key encryption key, whereby the interchip key is protected with the key encryption key outside the first chip package" is taught in '355 col. 1, lines 56-59.

As to dependent claim 43, "further comprising a step of overwriting the interchip key in the second key storage register from outside the second chip package" is shown in '489 col. 7, lines 15-19, overwriting same as replaced or changing keys to new host.

As to dependent claim 44, "further comprising steps of: encrypting the digital content in the second chip package to produce second ciphertext content using a second interchip key, coupling the second ciphertext content to a second content pathway" is disclosed in '489 col. 5, line 63 through col. 6, line 5.

As to dependent claim 45, "further comprising: providing a unique interchip key to each of a plurality of content processing chip packages, the unique interchip key of each content processing chip package being distinct from the unique key of each other content processing chip package and protecting a respective content pathway to each content chip processing package" is shown in '489 col. 7, lines 11-19, note because it is a manufacturing process there are a plurality of smart cards that are paired with a respective plurality of to a specific host Descrambler IC.

As to dependent claim 46, "wherein the step of providing a unique interchip key includes providing a message to each of the plurality of content processing chip packages,

and each content processing chip package decrypts the message to obtain a unique interchip key" is disclosed in '489 col. 7, lines 15-19.

As to dependent claim 53, "wherein the interchip key in the first key storage register is rendered into a non-readable from outside the first chip package by activating a feature of the first chip package that prevents overwriting the interchip key in the first key storage register from outside the first chip package, after a period in which the first key is loaded in the first key storage" is taught in '355 col. 4, lines 8-52.

As to independent claim 47, this claim is directed a computer readable medium containing instructions for a computer to perform a method of independent claim 41; therefore it is rejected along similar rationale.

As to dependent claims 48-52 and 54, these claims contain substantially similar subject matter as claims 42-47 and 53; therefore they are rejected along similar rationale.

Conclusion

14. It is noted, PATENTS ARE RELEVANT AS PRIOR ART FOR ALL THEY CONTAIN "The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain." In re Heck, 699 F.2d 1331, 1332-33, 216 USPQ 1038, 1039 (Fed. Cir. 1983) (quoting In re Lemelson, 397 F.2d 1006, 1009, 158 USPQ 275, 277 (CCPA 1968)). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments (see MPEP 2123).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ellen C Tran whose telephone number is (571) 272-3842. The examiner can normally be reached from 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached at (571) 272-7304. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/ELLEN TRAN/
Primary Examiner, Art Unit 2433
10 December 2010